

**SEMICONDUCTOR DEVICE**

Patent Number: JP61117858  
Publication date: 1986-06-05  
Inventor(s): TAKAHASHI HIDEKAZU  
Applicant(s): HITACHI MICRO COMPUT ENG LTD; others: 01  
Requested Patent: ☐ JP61117858  
Application JP19840238387 19841114  
Priority Number(s):  
IPC Classification: H01L25/08  
EC Classification:  
Equivalents:

**Abstract**

**PURPOSE:**To obtain a function of a plurality of ICs with one IC area by a method wherein semiconductor chips are provided in a stack in the same package.

**CONSTITUTION:**A semiconductor chip 2 is provided on the tab 1 of the upper stage, and the terminals of the chips 2 are bonded to the tips of inner leads 3, 4 with Au wires 5, 6 or the like. A semiconductor chip 12 is provided on the tab 11 of the lower stage, and the terminals of the chip 12 are bonded to the tips of inner leads 13, 14 with Au wires 15, 16 or the like. The other ends of the inner leads are outer leads 8, 9, 18, 19. Providing the semiconductor chips 2, 12 in the same package 17 not only makes double integration degrees but also enables mounting as one IC. The semiconductor chips may have either the same function or different functions in the same manner as the digital IC and the analog IC. Thus, the mounting area can be substantially reduced largely.

Data supplied from the esp@cenet database - 12